WHAT IS CLAIMED IS:

1. A semiconductor circuit device having an active state and a standby state, comprising:

a first main power supply line receiving a first power supply voltage;

a first sub power supply line;

a first switching element connected between said first main power supply line and said first sub power supply line, turned on in said active state and turned off in said standby state;

a second main power supply line receiving a second power supply voltage;

a first logic circuit connected between said second main power supply line and said first sub power supply line and outputting a first logical level corresponding to said second power supply voltage in said standby state; and

a first constant current circuit disposed to supply a constant current to said first sub power supply line.

2. The semiconductor circuit device according to claim 1, further comprising:

a second sub power supply line,

a second switching element connected between said second main power supply line and said second sub power supply line, turned on in said active state and turned off in said standby state,

a second logic circuit connected between said first main power supply line and said second sub power supply line and outputting a second logical level corresponding to said first power supply voltage in said standby state, and

a second constant current circuit disposed to supply a constant current to said second sub power supply line.

3. A semiconductor circuit device having an active state and a standby state, comprising:

a main power supply line receiving a power supply voltage;

a sub power supply line;

a first switching element connected between said main power supply line and said sub power supply line, turned on in said active state and turned off in said standby state;

a main ground line receiving a ground voltage;

a sub ground line;

a second switching element connected between said main ground line and said sub ground line, turned on in said active state and turned off in said standby state;

a first logic circuit connected between said main power supply line and said sub ground line and outputting a logical high level in said standby state;

a second logic circuit connected between said sub power supply line and said main ground line and outputting a logical low level in said standby state;

a first constant current circuit disposed to supply a constant current to said sub power supply line; and

a second constant current circuit disposed to supply a constant current to said sub ground line.

4. The semiconductor circuit device according to claim 3, wherein said first constant current circuit includes:

a first charge circuit disposed to charge said sub power supply line,

a first monitor circuit disposed to monitor a current supplied from said first charge circuit to said sub power supply line, and

a first control circuit disposed to control said first charge circuit so as to keep said current monitored by said first monitor circuit constant, and

said second constant current circuit includes:

a second charge circuit disposed to charge said sub ground line,

a second monitor circuit disposed to monitor a current supplied from said second charge circuit to said sub ground line, and

a second control circuit disposed to control said second charge circuit

so as to keep said current monitored by said second monitor circuit constant.

5. The semiconductor circuit device according to claim 4, wherein said first monitor circuit monitors a current flowing in said main ground line, and

said second monitor circuit monitors a current flowing in said main power supply line.

6. The semiconductor circuit device according to claim 5, wherein said first monitor circuit includes a first resistance element inserted into said main ground line,

said first control circuit includes a first differential amplifier receiving a voltage generated across said first resistance element and having an offset voltage,

said first charge circuit includes a first transistor having a gate receiving an output voltage of said first differential amplifier,

said second monitor circuit includes a second resistance element inserted into said main power supply line,

said second control circuit includes a second differential amplifier receiving a voltage generated across said second resistance element and having an offset voltage, and

said second charge circuit includes a second transistor having a gate receiving an output voltage of said second differential amplifier.

7. The semiconductor circuit device according to claim 4, wherein said first monitor circuit monitors a current flowing in said sub power supply line, and

said second monitor circuit monitors a current flowing in said sub ground line.

8. The semiconductor circuit device according to claim 7, wherein said first monitor circuit includes a first resistance element inserted into said sub power supply line,

said first control circuit includes a first differential amplifier receiving a voltage generated across said first resistance element and having an offset voltage,

said first charge circuit includes a first transistor having a gate receiving an output voltage of said first differential amplifier,

said second monitor circuit includes a second resistance element inserted into said sub ground line,

said second control circuit includes a second differential amplifier receiving a voltage generated across said second resistance element and having an offset voltage, and

said second charge circuit includes a second transistor having a gate receiving an output voltage of said second differential amplifier.

9. The semiconductor circuit device according to claim 8, further comprising:

a third differential amplifier receiving a voltage generated between said main power supply line and said sub power supply line and having an offset voltage,

a P-channel MOS transistor connected between said main power supply line and said sub power supply line and having a gate receiving an output voltage of said third differential amplifier,

a fourth differential amplifier receiving a voltage generated between said main ground line and said sub ground line and having an offset voltage, and

an N-channel MOS transistor connected between said main ground line and said sub ground line and having a gate receiving an output voltage of said fourth differential amplifier.

10. The semiconductor circuit device according to claim 3, wherein said first constant current circuit includes:

a first current mirror circuit having a first P-channel MOS transistor connected to said sub power supply line and a second P-channel MOS transistor connected to said first P-channel MOS transistor, and

a first current source connected to said second P-channel MOS transistor, and

said second constant current circuit includes:

a second current mirror circuit having a first N-channel MOS transistor connected to said sub ground line and a second N-channel MOS transistor connected to said first N-channel MOS transistor, and

a second current source connected to said second N-channel MOS transistor.

11. The semiconductor circuit device according to claim 10, further comprising:

a first differential amplifier receiving a voltage generated between said main power supply line and said sub power supply line and having an offset voltage,

a third P-channel MOS transistor connected between said first P-channel MOS transistor and said sub power supply line and having a gate receiving an output voltage of said first differential amplifier,

a second differential amplifier receiving a voltage generated between said main ground line and said sub ground line and having an offset voltage, and

a third N-channel MOS transistor connected between said first N-channel MOS transistor and said sub ground line and having a gate receiving an output voltage of said second differential amplifier.

12. The semiconductor circuit device according to claim 3, further comprising:

a short circuit disposed to short said sub power supply line and said sub ground line in said standby state.

13. The semiconductor circuit device according to claim 12, wherein said first switching element is a first P-channel MOS transistor and said second switching element is a first N-channel MOS transistor,

said semiconductor circuit device further comprises:

a short signal generation circuit disposed to generate a first short signal changing to a logical low level in said active state and changing to a logical high level in said standby state and supply the first short signal to a gate of said first P-channel MOS transistor and generating a second short signal complementary to said first short signal and supplying the second short signal to a gate of said first N-channel MOS transistor, and

said short circuit includes:

a second N-channel MOS transistor connected between said sub power supply line and said sub ground line and having a gate receiving said first short signal, and

a second P-channel MOS transistor connected between said sub power supply line and said sub ground line and having a gate receiving said second short signal.

14. A semiconductor circuit device having an active state and a standby state, comprising:

a main power supply line receiving a power supply voltage;

a sub power supply line;

a switching P-channel MOS transistor connected between said main power supply line and said sub power supply line, turned on in said active state and turned off in said standby state;

a main ground line receiving a ground voltage;

a sub ground line;

a switching N-channel MOS transistor connected between said main ground line and said sub ground line, turned on in said active state and turned off in said standby state;

a first logic circuit connected between said main power supply line and said sub ground line and outputting a logical high level in said standby state;

a second logic circuit connected between said sub power supply line and said main ground line and outputting a logical low level in said standby state;

a first back gate voltage supply circuit disposed to supply said power

supply a voltage to a back gate of said switching P-channel MOS transistor in said active state and supply a voltage higher than said power supply voltage to said back gate of said switching P-channel MOS transistor in said standby state; and

a second back gate voltage supply circuit disposed to supply said ground voltage to a back gate of said switching N-channel MOS transistor in said active state and supply a voltage lower than said ground voltage to said back gate of said N-channel MOS transistor in said standby state.

15. The semiconductor circuit device according to claim 14, further comprising:

a short signal generation circuit disposed to generate a first short signal changing to a voltage level higher than said power supply voltage in said active state and changing to a voltage level lower than said ground voltage in said standby state to supply the first short signal to a gate of said switching P-channel MOS transistor and generate a second short signal complementary to said first short signal to supply the second short signal to a gate of said switching N-channel MOS transistor, wherein

said first back gate voltage supply circuit includes a maximum value circuit connected to said main power supply line and said gate of said switching P-channel MOS transistor for selecting the higher one of said power supply voltage of said main power supply line and the voltage of said gate of said switching P-channel MOS transistor to supply the higher voltage to said back gate of said switching P-channel MOS transistor, and

said second back gate voltage supply circuit includes a minimum value circuit connected to said main ground line and said gate of said switching N-channel MOS transistor for selecting the lower one of said ground voltage of said main ground line and the voltage of said gate of said switching N-channel MOS transistor to supply the lower voltage to said back gate of said switching N-channel MOS transistor.

16. The semiconductor circuit device according to claim 15, wherein said maximum value circuit includes a first differential amplifier, a gate of

a first input N-channel MOS transistor of said first differential amplifier is connected to said main power supply line and a gate of a second input N-channel MOS transistor of said first differential amplifier is connected to an output node of said maximum value circuit,

said maximum value circuit further includes an N-channel MOS transistor connected in parallel with said first input N-channel MOS transistor of said first differential amplifier and having a gate connected to said gate of said switching P-channel MOS transistor,

said minimum value circuit includes a second differential amplifier, a gate of a first input P-channel MOS transistor of said second differential amplifier is connected to said main ground line and a gate of a second input P-channel MOS transistor of said second differential amplifier is connected to an output node of said minimum value circuit, and

said minimum value circuit further includes a P-channel MOS transistor connected in parallel with said first input P-channel MOS transistor of said second differential amplifier and having a gate connected to said gate of said switching N-channel MOS transistor.

17. A semiconductor circuit device including a first hierarchical block and a plurality of second hierarchical blocks,

said first hierarchical block including:

a first power supply system disposed to supply a voltage to an internal circuit in said first hierarchical block,

a first receiving circuit disposed to receive an externally supplied first request signal and activate said first power supply system, and

a plurality of transmission circuits corresponding to said plurality of second hierarchical blocks, each disposed to transmit a second request signal to corresponding said second hierarchical block, and

each said second hierarchical block including:

a second power supply system disposed to supply a voltage to an internal circuit in said second hierarchical block, and

a second receiving circuit disposed to receive said second request signal and activate said second power supply system.

18. The semiconductor circuit device according to claim 17, wherein said first receiving circuit returns a first response signal to an external device after said first power supply system is activated,

said second receiving circuit returns a second response signal to corresponding said transmission circuit after said second power supply system is activated, and

said internal circuit in said first hierarchical block activates/inactivates said second request signal in response to an externally supplied first command signal and supply a second command signal to said internal circuit in corresponding said second hierarchical block when one of said transmission circuits receives said second response signal.

19. The semiconductor circuit device according to claim 17, wherein said first receiving circuit inactivates said first power supply system when not receiving said first request signal after a lapse of a prescribed period from completion of an operation of said internal circuit in said first hierarchical block, and

said second receiving circuit inactivates said second power supply system when not receiving said second request signal after a lapse of a prescribed period from completion of an operation of said internal circuit in said second hierarchical block.

20. The semiconductor circuit device according to claim 17, wherein said internal circuit in said first hierarchical block transmits a command signal to said internal circuit in said second hierarchical block when a prescribed period elapses after said transmission circuit transmits said second request signal.